To: Technology Center: **2186**
Facsimile Number: **703-872-9306**

Total Pages Sent: 18

From: Robert D. Marshall, Jr.
Texas Instruments Incorporated
Facsimile: 972-917-4418
Phone: 972-917-5290

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of		TI-29030	
	Laurent Six, et al.	Art Unit: 2186	
Serial No.:	09/591,615	Examiner: Pierre Miche Bataille	
Filed:	June 9, 2000	Conf. No.: 2796	
For:	Shared Memory With Programmable Size		

CERTIFICATION OF FACSIMILE TRANSMISSION

I hereby certify that the following papers are being transmitted by facsimile to the U.S. Patent and Trademark Office at 703-872-9306 on the date shown below:

Robin E. Barnum — December 31, 2003
Date

FACSIMILE COVER SHEET

X	**FACSIMILE COVER SHEET**	___	AMENDMENT (# Pages)
___	NEW APPLICATION	___	EOT (# Pages)
___	DECLARATION (# Pages)	___	NOTICE OF APPEAL (Page)
___	ASSIGNMENT (# Pages)	X	**APPEAL Brief (16 Pages)**
___	FORMAL DRAWINGS	___	ISSUE FEE (# Pages)
___	INFORMAL DRAWINGS	___	REPLY BRIEF (IN TRIPLICATE) (# Pages)
___	CONTINUATION APP'N (# Pages)	X	**Appeal Brief Fee TL (1 page)**
___	DIVISIONAL APP'N		

NAME OF INVENTOR(S): Laurent Six, et al.	RECEIPT DATE & SERIAL NO.: **Serial No.: 09/591,615** **Filing Date:** June 9, 2000
TITLE OF INVENTION: Shared Memory With Programmable Size	
TI FILE NO.: **TI-29030** / DEPOSIT ACCT. NO.: **20-0668**	
FAXED: 12/31/03 DUE: 12/31/03 ATTY/SEC'Y: RDM/reb	

Texas Instruments Incorporated
PO Box 655474, M/S 3999
Dallas, TX 75265

U.S. PATENT AND TRADEMARK OFFICE
APPEAL BRIEF TRANSMITTAL FORM

TI-29030
Docket No.

CERTIFICATION OF FAX TRANSMITTAL I hereby certify that the above correspondence is being facsimile transmitted to the Patent and Trademark Office on **December 31, 2003**.

Robin E. Barnum

In re Application of

Laurent Six, et al.

Serial No: 09/591,615

Filed: June 9, 2000

For: Shared Memory With Programmable Size

Conf. No: 2796

01/09/2004 CBAHLER 00000015 09591615
01 FC:1402 330.00 DA

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Transmitted herewith is an Appeal Brief in the above-identified application.

Please charge the $320.00 fee for filing the Brief to Texas Instruments Incorporated, Deposit Account No. 20-0668.

Charge any additional fees, or credit overpayment to Texas Instruments Incorporated, Deposit Account No. 20-0668.

Texas Instruments Incorporated
P.O. Box 655474, MS 3999
Dallas, TX 75265
(972) 917-5290

Robert D. Marshall, Jr.
Attorney for Applicants
Registration No. 28,527

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Six et al
Art Unit: 2186
Serial No.: 09/591,615
Examiner: Pierre M. Bataille
Filed: June 9, 2000
Docket: TI-29030
For: SHARED MEMORY WITH PROGRAMMABLE SIZE

#11
C. Barnum
1/8/04

Appeal Brief under 37 C.F.R. §1.192

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

CERTIFICATION OF FAX TRANSMITTAL UNDER 37 C.F.R. §1.6(b)

I hereby certify that the above correspondence is being facsimile transmitted to the Patent and Trademark Office on December 31, 2003.

Robin E. Barnum

Dear Sir:

This is Appellant's Appeal Brief filed pursuant to 37 C.F.R. §1.192 and the Notice of Appeal filed October 31, 2003.

Real Party in Interest under 36 C.F.R. §1.192(c)(1)

The real party in interest in this application is Texas Instruments Incorporated, a corporation of Delaware with its principle place of business in Dallas, Texas. An assignment to Texas Instruments Incorporated is recorded at reel 010886 and frames 0529 to 0532.

Related Appeals and Interferences under 36 C.F.R. §1.192(c)(2)

There are no appeals or interferences related to this appeal in this application.

Status of the Claims on Appeal under 37 C.F.R. §1.192(c)(3)

The claims are claims 1 to 12. Claims 1 to 12 are rejected. No claims are allowed.

Status of Amendments Filed After Final Rejection under 37 C.F.R. §1.192(c)(4)

No amendments to the claims were proposed in the response filed September 30, 2003 following the FINAL REJECTION of August 1, 2003.

Summary of the Invention under 37 C.F.R. §1.192(c)(5)

The digital system of this invention includes a memory circuit, a first requestor circuit with a first memory access node and a second requestor circuit with a second memory access node. A scheduling circuit sequentially schedules memory accesses to the memory circuit by the first requestor circuit and by the second request circuit. A selection circuit is connected to the first memory access node and to the scheduling circuit request output node with an output node connected to the memory circuit. An access mode circuitry controls connection of the selection circuit for a first access mode and a second access mode. In the first access mode, both the first requestor circuit and the second requestor circuit can sequentially access the memory circuit. In the second access mode, the first requestor circuit has exclusive access to the memory circuit. A size register holds a size parameter and is coupled to the selection circuit. The selection circuit selects a first portion of the memory circuit in response to the size parameter when in the second access mode so that only

the first portion of the memory circuit is operable for exclusive access by the first requestor when in the second access mode.

The second portion of the memory circuit not selected in response to the size parameter is put into a low power mode when the access mode circuitry indicates the second access mode.

The second portion of the memory circuit not selected in response to the size parameter can be accessed by the second requestor in the second access mode.

The size parameter is ignored in the first access mode enabling the entire memory circuit to operate for sequential access by the first requestor and the second requestor.

The digital system further includes a clock circuit connected to the second requestor and the memory circuit. The first portion of the memory circuit operates synchronously with the clock circuit in the first access mode. The first portion of the memory circuit operates asynchronously in the second access mode.

The first requester circuit is a host processor and the second requester circuit is direct memory access circuit channel controller.

The digital system is a cellular telephone including an integrated keyboard, a display and radio frequency circuitry all connected to a microprocessor, and an aerial.

The method of this invention operates a digital system having a memory circuit that is shared by plural requestor circuits. The method shares access to the memory circuit between the plural requestor circuits in a first mode. The method selects a first portion of the memory circuit responsive to a size parameter stored in a register. A second portion of the memory circuit is not selected. The method limits access to the first portion of memory circuit to only a first requestor when in a second mode.

The method shares access to the second portion of the memory circuit between the plural requestor circuits when in the second.

The method places the second portion of the memory circuit in a low power mode when in the second mode.

The memory has a total size equal to the sum of the first portion and the second portion.

The method stores a different size parameter in the register. The method selects a first portion having a different size in response to the different size parameter.

Statement of Issues Presented for Review under 37 C.F.R. §1.192(c)(6)

(1) Are claims 1 to 7 made obvious under 35 U.S.C. 103(a) by the combination of Boutaud et al U.S. Patent No. 5,838,934 and Pawate et al U.S. Patent No. 5,638,530?

(2) Are claims 8 to 12 anticipated under 35 U.S.C. 102(b) by Pawate et al U.S. Patent No. 5,638,530?

Statement of the Grouping of Claims under 37 C.F.R. §1.192(c)(7)

The Applicants respectfully submit that the claims of this application are independently patentable in the following groups:

Group I: claim 1, claims 5, 6 and 7 are grouped with claim 1;
Group II: claim 2;
Group III: claim 3;
Group IV: claim 4;
Group V: claim 8;
Group VI: claim 9; and
Group VII: claim 10.

This Appeal Brief includes separate arguments for each of these groups. In accordance with the procedure sanctioned in

MPEP §1206(5) the Appellant respectfully submits these separate arguments fulfill the requirement of 37 C.F.R. §1.192(c)(6) for statement of the reason why the claims are believed separately patentable.

Arguments

Rejection (1)

Group I

Claim 1 recites subject matter not made obvious by the combination of Boutaud et al and Pawate et al. Claim 1 recites "both the first requestor circuit and the second requestor circuit can sequentially access the memory circuit when the access mode circuitry indicates the first access mode." The FINAL REJECTION at page 10, lines 10 to 13 states that the claimed first access mode corresponds to the smart card standard mode taught in Pawate et al. Pawate et al states at column 6, lines 48 to 50:

> "While the smart card (100) is in the standard mode, the DSP (170) is inactive, and this is the default mode of the smart card."

The Applicants respectfully submit that the DSP (170) of Pawate et al cannot access the shared memory as required by the above quoted language of claim 1 if the DSP is inactive. Accordingly, claim 1 is unobvious over Boutaud et al and Pawate et al.

Regarding this limitation, the FINAL REJECTION states at page 10, lines 14 to 21:

> "selecting a portion of the memory (attribute memory 160 of the smart card) responsive to a size parameter stored in a register (interface configuration registers 130) [Col. 4, Lines 53-65], such that the second portion is not selected (common memory 150 of the smart card) [Col. 7, Lines 36-42]; and limiting access (smart mode) to the first portion of the

> memory circuit (attribute memory 160 of the smart card) to only a first requestor (digital signal processor (DSP) 170) in a second mode of operation (smart mode) [Col. 13, Lines 53-65; Col. 14, Lines 32-41; Col. 7, Lines 22-42, Col. 7, Line 61 to Col. 8, Line 2]."

The Applicants wish to point out that none of the portions of Pawate et al cited in this paragraph of the FINAL REJECTION (Col. 13, Lines 53-65; Col. 14, Lines 32-41; Col. 7, Lines 22-42, Col. 7, Line 61 to Col. 8, Line 2) include any mention of common memory 150 or attribute memory 160. Thus these portions of Pawate et al cannot make obvious the differing access to these two memories recited in claim 1. Accordingly, claim 1 is unobvious over Boutaud et al and Pawate et al.

Claim 1 recites further subject matter not made obvious by the combination of Boutaud et al and Pawate et al. Claim 1 recites "select a first portion of the memory circuit in response to the size parameter when the access mode circuitry indicates the second access mode, wherein only the first portion of the memory circuit is operable for exclusive access by the first requestor when the access mode circuitry indicates the second access mode." Pawate et al has no such teaching or suggestion to select a first portion of memory in accordance with a size parameter and to limit access to the selected portion. Pawate et al states at column 13, lines 29 to 35:

> "Since both the DSP and the host computer access the shared memory on the smart card, bus arbitration is necessary. If the host computer attempts to access the shared memory, the operation of the DSP is halted."

Thus Pawate et al clearly teaches that arbitration is required unless the DSP is turned off. Pawate et al states at column 13, lines 49 to 52:

> "If the CLKON bit is set to zero, the DSP (120) is placed in a hold state, forcing the buses of the DSP (170) to be tri-stated and allowing the host computer to have free access to the common memory (150)."

Pawate et al does teach use of a control register that provides limited access. Pawate et al states at column 13, lines 35 to 39:

> "However, since the communication control and control registers are not resident in the shared memory, but in fact are resident in the interface and control circuit (180), access, write or read to these registers by the host computer does not halt the operation of the DSP."

Pawate et al states these control registers are not in the shared memory. Thus these control registers are not relevant to the present claims. Pawate et al has no teaching or suggestion to select a first portion of memory in accordance with a size parameter and to limit access to the selected portion, as recited in Claim 1. Likewise, Boutaud et al has no such teaching. Boutaud et al does have a shared access mode (SAM) and a host only mode (HOM). Boutaud et al teaches at column 8, line 59 to column 9, line 7 that the entire memory circuit 200 is treated as a single portion and is either entirely in host only mode or in shared access mode. Neither Boutaud et al nor Pawate et al suggest "a size register for holding a size parameter coupled to the selection circuit, the selection circuit being operable to select a first portion of the memory circuit in response to the size parameter when the access mode circuitry indicates the second access mode, wherein only the first portion of the memory circuit is operable for exclusive access by the first requestor when the access mode circuitry indicates the second access mode" as recited in Claim 1. Claim 1 is therefore allowable over the combination of Boutaud et al and Pawate et al.

Group II

Claim 2 recites subject matter not made obvious by the combination of Boutaud et al and Pawate et al. Claim 2 recites "a second portion of the memory circuit not selected in response to the size parameter is operable to be in a low power mode when the access mode circuitry indicates the second access mode." Pawate et al does not teach placing the second portion of the memory circuit in a low power mode when the access mode circuitry indicates the second mode of operation. Pawate et al instead teaches powering down the DSP corresponding to the claimed second requestor circuitry. The FINAL REJECTION cites column 14, lines 3 to 13 of Pawate et al as teaching this powering down of the second portion of the memory. This portion of Pawate et al states:

> "Next, the host computer enables the AFEINT by setting the AINTEN bit allowing the host computer to be interrupted by the AFE card, for example, by the voice activated switch or the ring detect. The host computer now may reduce power consumption of the system and turn off the clock of the DSP by setting the CLKON bit to zero. The DSP (170) is placed into a hold mode and tri-stating the buses of the DSP, allowing the host computer to have quicker access to the remaining unused portion on the card (100). When the desired or expected external event occurs as indicated by the AFEINT, the host computer turns the clock of the DSP on and the DSP (170) begins executing the algorithm."

Thus Pawate et al teaches "turn off the clock of the DSP" to minimize power. This corresponds to turning off one of the requestor circuits of base claim 1. This is a different structure than the second portion of memory recited in claim 2. Pawate et al does not suggest powering down a portion of the memory since the host is given access to the entire memory when the DSP is powered down. Claim 2 is therefore allowable over the combination of Boutaud et al and Pawate et al.

Group III

Claim 3 recites subject matter not made obvious by the combination of Boutaud et al and Pawate et al. Claim 3 recites "a second portion of the memory circuit not selected in response to the size parameter can be accessed by the second requestor when the access mode circuitry indicates the second access mode." The FINAL REJECTION cites column 13, lines 53 to 65 of Pawate et al as making obvious this limitation. Pawate et al states at column 13, lines 53 to 65:

> "The first kilobytes of the shared memory the host computer cannot access while the card is in the first mode.
>
> While in the smart mode, the host computer cannot access, by reading and writing, the first 2K bytes of the shared memory. Thus, these first two kilobytes of memory could be used as protected memory for the DSP. However, if the host computer accesses this protected block, the DSP is not put into a hold state. The host computer must load the reset and interrupt vectors of the DSP and the application program prior to switching the card into the smart mode. Since the host computer can access the entire memory on the card without consideration of the page sizes of the DSP (170), the memory pages not used by the DSP can be dedicated exclusively for use by the host computer. "

The Applicants respectfully submit that the language "The first kilobytes of the shared memory the host computer cannot access while the card is in the first mode" and "the host computer cannot access, by reading and writing, the first 2K bytes of the shared memory" must not be read as absolutes. Instead of indicating a hardware prohibition, these portions of Pawate et al must be understood as programming "should nots." Any other understanding of these disclosures cannot be reconciled with the language "if the host computer accesses this protected block" and "the host computer can access the entire memory on the card." Since the portion of Pawate et al cited in the FINAL REJECTION contradicts the premise

for which it is cited, this does not make the limitation obvious. Accordingly, claim 3 is allowable over the combination of Boutaud et al and Pawate et al.

Group IV

Claim 4 recites subject matter not made obvious by the combination of Boutaud et al and Pawate et al. Claim 4 recites "the size parameter is ignored when the access mode circuitry indicates the first access mode such that the entire memory circuit is operable to be selected for sequential access by the first requestor and the second requestor." Neither Pawate et al nor Boutaud et al suggest a size parameter for selecting a portion of the memory. Thus neither can suggest ignoring the size parameter as recited in claim 4. Accordingly, claim 4 is allowable over the combination of Boutaud et al and Pawate et al.

Rejection (2)

Group V

Claim 8 recites subject matter not anticipated by Pawate et al. Claim 8 recites "selecting a first portion of the memory circuit responsive to a size parameter stored in a register, such that a second portion of the memory circuit is not selected; and limiting access to the first portion of memory circuit to only a first requestor of the plurality of requestors when the digital system is in a second mode of operation." Pawate et al has no such teaching or suggestion to select a first portion of memory in accordance with a size parameter and to limit access to the selected portion. Pawate et al states at column 13, lines 29 to 35:

> "Since both the DSP and the host computer access the shared memory on the smart card, bus arbitration is necessary. If the

> host computer attempts to access the shared memory, the operation of the DSP is halted."

This clearly teaches that arbitration is required unless the DSP is turned off. Pawate et al states at column 13, lines 49 to 52:

> "If the CLKON bit is set to zero, the DSP (120) is placed in a hold state, forcing the buses of the DSP (170) to be tri-stated and allowing the host computer to have free access to the common memory (150)."

Pawate et al does teach use of a control register that provides limited access. Pawate et al states at column 13, lines 35 to 39:

> "However, since the communication control and control registers are not resident in the shared memory, but in fact are resident in the interface and control circuit (180), access, write or read to these registers by the host computer does not halt the operation of the DSP."

These control registers are not shared and are not relevant to the present claims. Therefore, Claim 8 is allowable over Pawate et al.

Group V

Claim 9 recites subject matter not anticipated by Pawate et al. Claim 9 recites "sharing access to the second portion of the memory circuit between the plurality of requestor circuits when the digital system is in the second mode of operation." Pawate et al states at column 6, lines 47 to 49:

> "While the smart card is in the standard mode, the DSP is inactive."

Pawate et al also reaches at column 13, line 30 while in smart mode, "bus arbitration is necessary." Thus, Pawate et al does not suggest a mode where a first portion of the memory is limited to one requester while the second portion is shared. Claim 9 is therefore allowable over Pawate et al.

Group VII

Claim 10 recites subject matter not anticipated by Pawate et al. Claim 10 recites "placing the second portion of the memory circuit in a low power mode when the digital system is in the second mode of operation." Pawate et al does not teach placing the second portion of the memory circuit in a low power mode when the digital system is in the second mode of operation. Instead, Pawate et al teaches at column 14, lines 6 to 8 "turn off the clock of the DSP" to minimize power. This power down disclosed in Pawate et al is of a different structure than claimed. Pawate et al does not suggest powering down a portion of the memory since the host is given access to the memory when the DSP is powered down. Claim 10 is therefore allowable over Pawate et al.

If the Examiner has any questions or other correspondence regarding this application, Applicants request that the Examiner contact Applicants' attorney at the below listed telephone number and address to facilitate prosecution.

Texas Instruments Incorporated
P.O. Box 655474 M/S 3999
Dallas, Texas 75265
(972) 917-5290
Fax: (972) 917-4418

Respectfully submitted,

Robert D. Marshall, Jr.
Reg. No. 28,527

APPENDIX

CLAIMS ON APPEAL

1. A digital system, comprising:

a memory circuit;

a first requestor circuit with a first memory access node;

a second requestor circuit with a second memory access node;

a scheduling circuit connected to the first memory access node and to the second memory access node and having a request output node, operable to sequentially schedule memory accesses to the memory circuit by the first requestor circuit and by the second request circuit;

a selection circuit connected to the first memory access node and to the scheduling circuit request output node with an output node connected to the memory circuit;

access mode circuitry for indicating at least a first access mode and a second access mode controllably connected to the selection circuit, such that both the first requestor circuit and the second requestor circuit can sequentially access the memory circuit when the access mode circuitry indicates the first access mode and the first requestor circuit has exclusive access to the memory circuit when the access mode circuitry indicates the second access mode; and

a size register for holding a size parameter coupled to the selection circuit, the selection circuit being operable to select a first portion of the memory circuit in response to the size parameter when the access mode circuitry indicates the second access mode, wherein only the first portion of the memory circuit is operable for exclusive access by the first requestor when the access mode circuitry indicates the second access mode.

2. The digital system of Claim 1, wherein a second portion of the memory circuit not selected in response to the size parameter is operable to be in a low power mode when the access mode circuitry indicates the second access mode.

3. The digital system according to Claim 1, wherein the selector circuit is operable such that a second portion of the memory circuit not selected in response to the size parameter can be accessed by the second requestor when the access mode circuitry indicates the second access mode.

4. The digital system according to Claim 1, wherein the size parameter is ignored when the access mode circuitry indicates the first access mode such that the entire memory circuit is operable to be selected for sequential access by the first requestor and the second requestor.

5. The digital system according to Claim 1, further comprising a clock circuit connected to the second requestor and to the memory circuit, wherein the first portion of the memory circuit operates synchronously with the clock circuit when the access mode circuitry indicates the first access mode and wherein the first portion of the memory circuit operates in an asynchronous manner when the access mode circuitry indicates the second access mode.

6. The digital system according to Claim 1, wherein the first requester circuit is a host processor and the second requester circuit is direct memory access circuit channel controller.

7. The digital system according to Claim 1 being a cellular telephone wherein one of the requestors is a microprocessor, further comprising:
an integrated keyboard (12) connected to the microprocessor via a keyboard adapter;
a display (14), connected to the microprocessor via a display adapter;
radio frequency (RF) circuitry (16) connected to the microprocessor; and
an aerial (18) connected to the RF circuitry.

8. A method of operating a digital system having a memory circuit that is shared by a plurality of requestor circuits, comprising the steps of:
sharing access to the memory circuit between the plurality of requestor circuits when the digital system is in a first mode of operation;
selecting a first portion of the memory circuit responsive to a size parameter stored in a register, such that a second portion of the memory circuit is not selected; and
limiting access to the first portion of memory circuit to only a first requestor of the plurality of requestors when the digital system is in a second mode of operation.

9. The method of Claim 8, further comprising the step of sharing access to the second portion of the memory circuit between the plurality of requestor circuits when the digital system is in the second mode of operation.

10. The method of Claim 8, further comprising the step of placing the second portion of the memory circuit in a low power mode when the digital system is in the second mode of operation.

11. The method of Claim 8, wherein the memory has a total size equal to the sum of the first portion and the second portion.

12. The method of Claim 11, further comprising the step of storing a different size parameter in the register, such that the step of selecting results in a first portion having a different size in response to the different size parameter.